a metal layer formed on said aluminum layer and made of any one material of tantalum, nickel, palladium, and molybdenum.

**2**. The semiconductor device according to claim **1**, wherein said n-type semiconductor layer or said undoped semiconductor layer is a III-V group nitride compound semiconductor layer.

**3**. The semiconductor device according to claim **1**, comprising a compound layer of any one material of tantalum, nickel, palladium, and molybdenum, and aluminum between said aluminum layer and said metal layer.

**4**. The semiconductor device according to claim **1**, comprising an $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) layer as said n-type semiconductor layer or said undoped semiconductor layer and a source electrode and a drain electrode as said ohmic electrode, and being a field effect transistor having a gate electrode.

**5**. The semiconductor device according to claim **4**, wherein:

said $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) layer is an $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer; and

comprising:

a GaN electron transit layer formed below said $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer; and

a GaN layer formed between said gate electrode and said $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer.

**6**. The semiconductor device according to claim **5**, wherein said GaN layer is doped with n-type impurity materials of $1 \times 10^{17}$ $cm^{-3}$ or more.

**7**. The semiconductor device according to claim **5**, further comprising a GaN layer below said source electrode and said drain electrode,

wherein said GaN layer is thinner in thickness at a portion below said source electrode and said drain electrode than at a portion below said gate electrode.

**8**. The semiconductor device according to claim **5**, wherein said $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 1$) electron supply layer is thinner in thickness at a portion below said source electrode and said drain electrode than at a portion below said gate electrode.

**9**. The semiconductor device according to claim **1**, wherein said substrate is a silicon carbide substrate having a resistivity of $1 \times 10^6$ Ω·cm or more.

**10**. The semiconductor device according to claim **1**, wherein said substrate is a conductive substrate having a resistivity of $1 \times 10^5$ Ω·cm or less.

**11**. A method for manufacturing a semiconductor device, comprising the steps of:

forming at least an n-type semiconductor layer or an undoped layer on a substrate;

forming a tantalum layer, an aluminum layer, and a metal layer made of any one material of tantalum, nickel, palladium, and molybdenum in order on said n-type semiconductor layer or said undoped semiconductor layer; and

annealing at temperatures lower than 600° C.

* * * * *